BI-FET II™ Technology

Quad SPST JFET Analog Switches

LF11331/LF13331 4 Normally Open Switches with Disable
LF11332/LF13332 4 Normally Closed Switches with Disable
LF11333/LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201/LF13201 4 Normally Closed Switches
LF11202/LF13202 4 Normally Open Switches

General Description

These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

Features

- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

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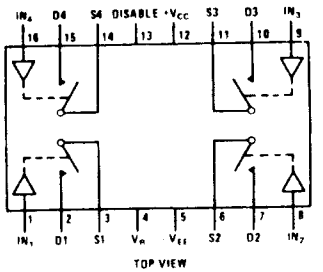
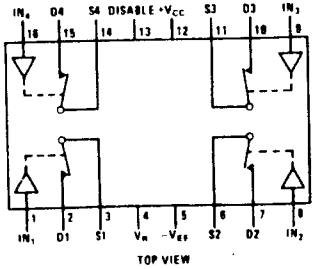
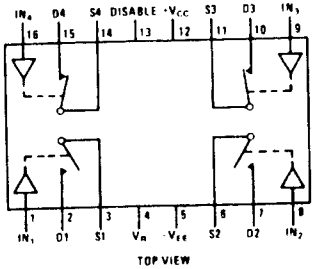
LF11331/LF13331



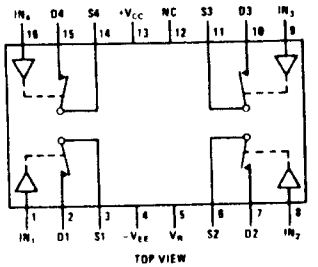
LF11332/LF13332



LF11333/LF13333



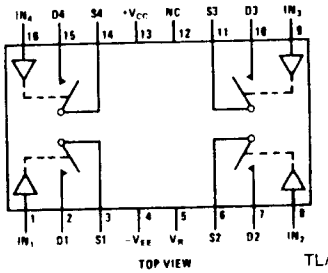
LF11201/LF13201



Order Number LF11201D, LF13201D, LF11202D, LF13202D, LF11331D, LF13331D, LF11332D, LF13332D, LF11333D, or LF13333D
See NS Package D16C

Order Number LF13201N, LF13202N, LF13331N, LF13332N, or LF13333N See NS Package N16A

LF11202/LF13202



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Test Circuit and Schematic Diagram

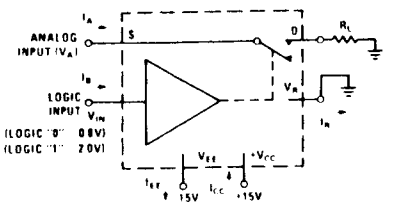

FIGURE 1. Typical Circuit for One Switch

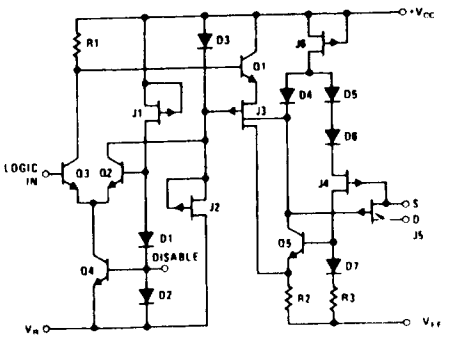

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FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

Positive Supply—Negative Supply ($V_{CC}-V_{EE}$)	36V
Reference Voltage	$V_{EE} \le V_R \le V_{CC}$
Logic Input Voltage	$V_R - 4.0V \le V_{IN} \le V_R + 6.0V$
Analog Voltage	$V_{EE} \le V_A \le V_{CC} + 6V$; $V_A \le V_{EE} + 36V$
Analog Current	$\|I_A\| < 20$ mA
Power Dissipation (Note 1)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	−55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		LF11331/2/3 LF11201/2			LF13331/2/3 LF13201/2			Units
				Min	Typ	Max	Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_A = 0$, $I_D = 1$ mA	$T_A = 25°C$		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		$T_A = 25°C$		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," $V_S = V_D = \pm 10V$	$T_A = 25°C$		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," $V_S = +10V$, $V_D = -10V$	$T_A = 25°C$		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," $V_S = +10V$, $V_D = -10V$	$T_A = 25°C$		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	$V_{IN} = 5V$	$T_A = 25°C$		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	$V_{IN} = 0.8$	$T_A = 25°C$			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	$V_S = \pm 10V$, (*Figure 3*)	$T_A = 25°C$		500			500		ns
t_{OFF}	Delay Time "OFF"	$V_S = \pm 10V$, (*Figure 3*)	$T_A = 25°C$		90			90		ns
$t_{ON} - t_{OFF}$	Break-Before-Make	$V_S = \pm 10V$, (*Figure 3*)	$T_A = 25°C$		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," $V_S = \pm 10V$	$T_A = 25°C$		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," $V_D = \pm 10V$	$T_A = 25°C$		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," $V_S = V_D = 0V$	$T_A = 25°C$		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	(*Figure 4*), (Note 3)	$T_A = 25°C$		−50			−50		dB
CT	Crosstalk	(*Figure 4*), (Note 3)	$T_A = 25°C$		−65			−65		dB
SR	Analog Slew Rate	(Note 4)	$T_A = 25°C$		50			50		V/μs
I_{DIS}	Disable Current	(*Figure 5*), (Note 5)	$T_A = 25°C$		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," $V_S = \pm 10V$	$T_A = 25°C$		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," $V_S = \pm 10V$	$T_A = 25°C$		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," $V_S = \pm 10V$	$T_A = 25°C$		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at ±100°C/W.

Note 2: Unless otherwise specified, $V_{CC} = +15V$, $V_{EE} = -15V$, $V_R = 0V$, and limits apply for $-55°C \le T_A \le +125°C$ for the LF11331, 2, 3 and the LF11202, 2, $-25°C \le T_A \le +85°C$ for the LF13331, 2, 3 and the LF13201,2.

Note 3: These parameters are limited by the pin to pin capacitance of the package.

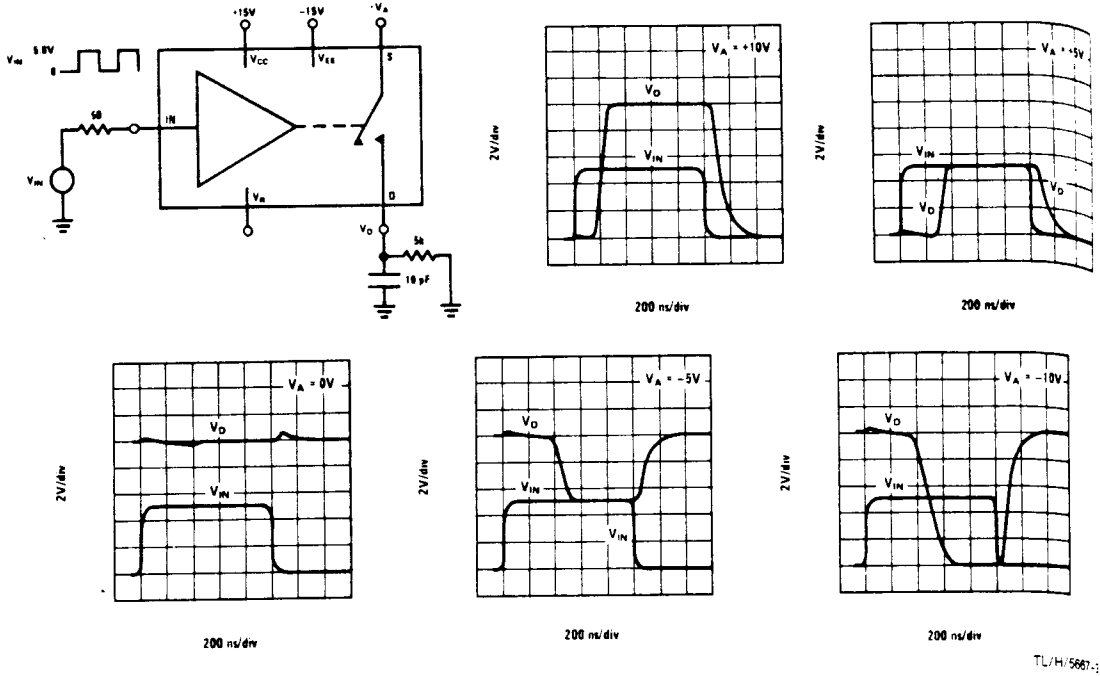
Note 4: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 5: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay time will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Note 6: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



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Additional Test Circuits

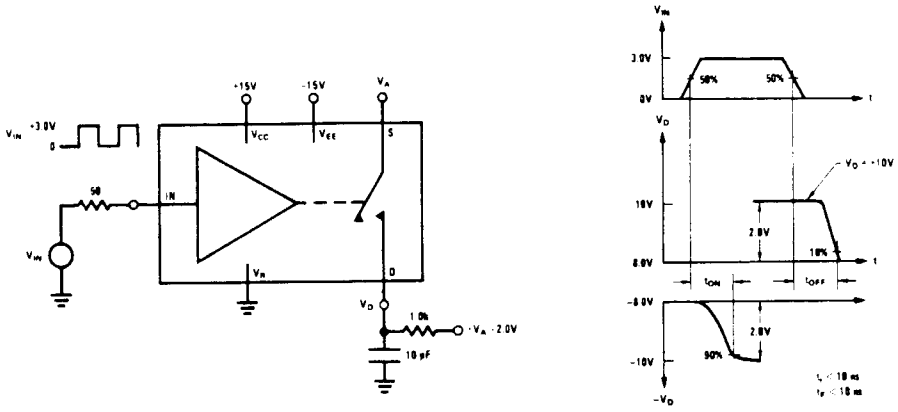

FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch

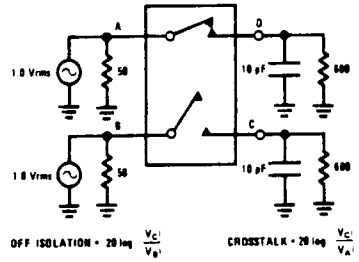

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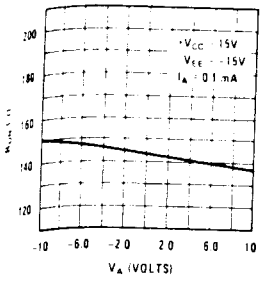
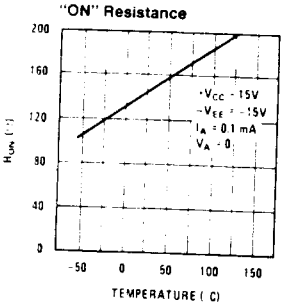
FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

Typical Performance Characteristics

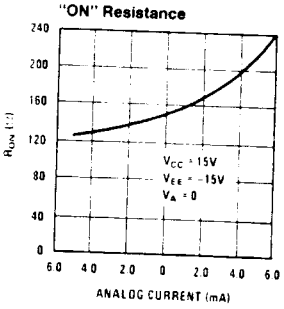
"ON" Resistance



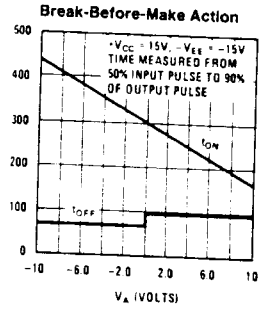
"ON" Resistance



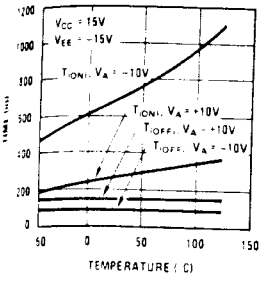
"ON" Resistance



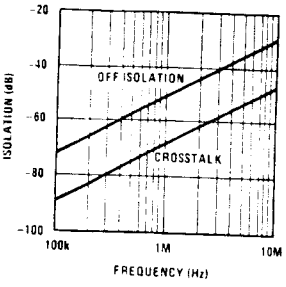
Break-Before-Make Action



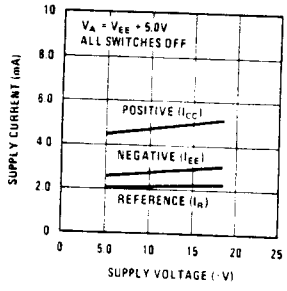
Switching Times



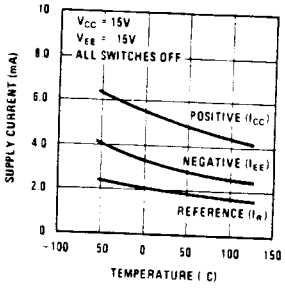
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



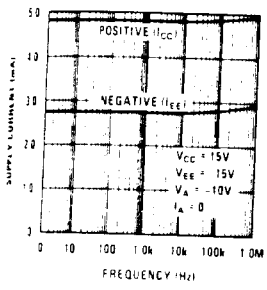
Supply Current



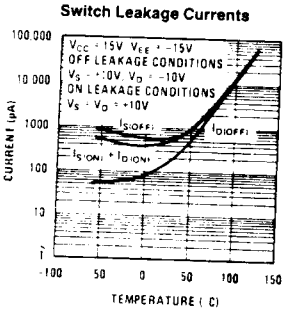
Supply Current



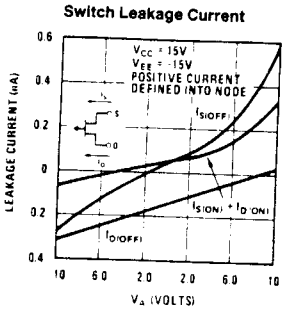
Supply Current



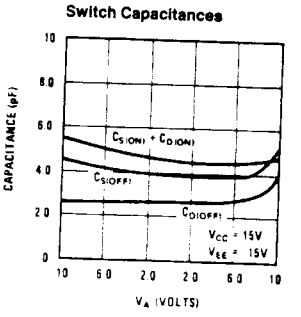
Switch Leakage Currents



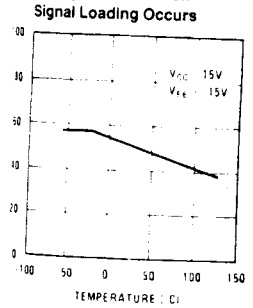
Switch Leakage Current



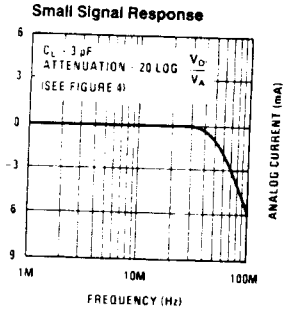
Switch Capacitances



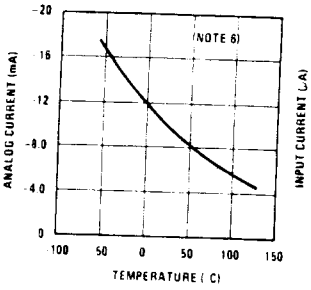
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



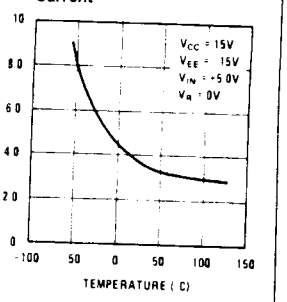
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



TL/H/5667–5

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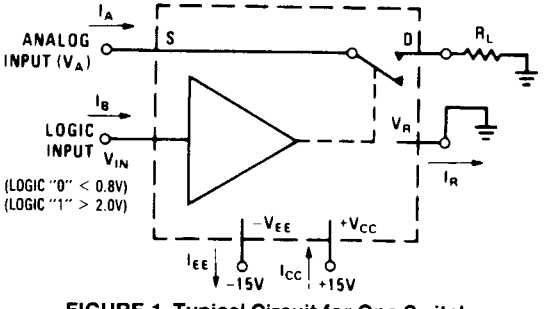

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FIGURE 1. Typical Circuit for One Switch

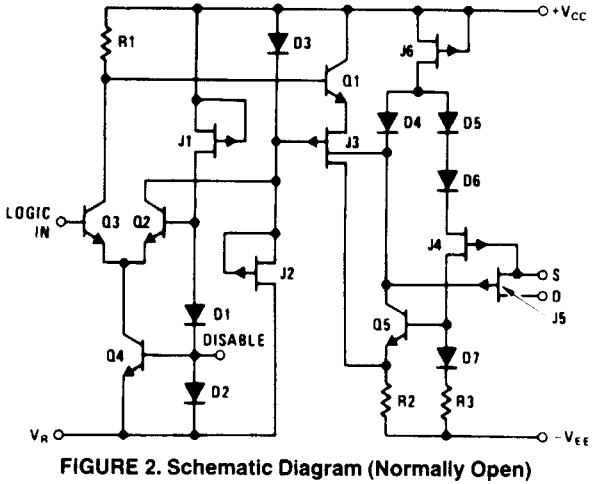

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FIGURE 2. Schematic Diagram (Normally Open)